IMP2A

3U CompactPCI Processor

PowerPact™3 CompactPCI

- High performance 3U CompactPCI processor
- CompactPCI system slot or peripheral slot
- PowerPC 7448 to 1.4 GHz
- Onboard PCI-X capable PMC site
- 1 MByte on-chip L2 cache
- Up to 512 MBytes DDR SDRAM
- 128 MBytes Flash
- Two fast sync/async serial ports
- Two 10/100/1000 Base-T Ethernet ports
- Up to 12 bits GPIO

RADSTONE DIGITAL PROCESSING

Designed for demanding applications with restrictive dimensional requirements, IMP2A packs a powerful SBC into an extremely space-efficient 3U form factor. IMP2A offers a seamless technology insertion opportunity for existing IMP1A users and an ultra-high performance entry point for new users.

IMP2A's impressive processing core is based around a Freescale 7448 PowerPC processor and a Marvell Discovery 3 Integrated System Controller which combines high bandwidth memory control and PCI bridging with an array of communication peripherals, including high speed serial and Ethernet ports, all on a single chip.

A range of I/O options is offered including up to two Gigabit Ethernet channels, up to 12 bits of discrete digital I/O, and up to two serial channels capable of high speed operation in either asynchronous or synchronous mode and software programmable as RS232/422 or 485.

IMP2A is fully supported by Radstone's Deployed Test software and a range of BSP support for standard COTS operating systems.

Features

System or peripheral slot	Support for up to seven peripheral slots	IMP2A detects a backplane signal to configure in system slot or peripheral slot mode
Processor	PowerPC 7448	The 7448 is Freescale's highest performance processing core. Typical power consumption for SBC = 15.0 Watts
System controller	Marvell 'Discovery' GT-64460	The Marvell Discovery 3 Integrated System Controller (ISC) combines a high bandwidth memory controller, two PCI-X interfaces and a range of communications peripherals, all on a single chip
L2 cache	1 MByte with ECC	Runs at core speed and is ECC supported
Main memory	Up to 512 MBytes DDR SDRAM with ECC	The CPU is interfaced to the main memory via a 64-bit data bus running at 133 MHz
Flash memory	128 MBytes Flash	The CPU is interfaced to the Flash memory via a 32-bit data bus running at 133 MHz. 128 MBytes are fitted as standard with 8 MBytes allocated to Boot Flash and 120 MBytes to user Flash
Non-volatile RAM	128 KBytes NVRAM	Non-volatile RAM combines the advantages of SRAM (fast read and write) and EPROM (non-volatility and in-circuit programmability) providing non-volatile storage for data which must not be lost when power is removed
Real-time clock	One second resolution	The RTC provides TOD/calendar with one second resolution. Standby power must be connected to maintain data during power down
Ethernet interfaces	10/100/1000 Base-T one or two ports	One or two Ethernet channels are provided from the Discovery 3 ISC and can be accessed through the J2 connector (See Fig. 2 for I/O options)
Serial ports	RS232/422/485 two ports async/sync	Two serial channels are provided from the Discovery 3 ISC. Both channels are software-selectable to be RS232/422 or 485 (see Fig. 2 for I/O options)
Discrete digital I/O	12 bits	Up to 12 bits of TTL compatible discrete digital I/O are provided from the Discovery ISC, each bit being capable of generating an interrupt. (See Fig. 2 for I/O options)
Timers	4- x 32-bit timers	Timers are provided from the Discovery 3 ISC
Watchdog timer	Programmable 32-bit timer	Watchdog timer provided by the Discovery 3 ISC
CompactPCI interface	32-bit/66 MHz 3.3 Volts (5 Volts tolerant	A 32-bit/66 MHz cPCI interface is provided conforming to the mechanical definitions of VITA 30.
DMA controllers	Six available	Six DMA controllers are available in the Discovery 3 ISC for efficiently moving large blocks of data
Elapsed time indicator	Quarter second resolution	The ETI logs the total accumulated time the SBC has been powered, with quarter second resolution, and the number of power cycles
JTAG interface	-	A JTAG header is accessible for both factory test and software de-bug purposes

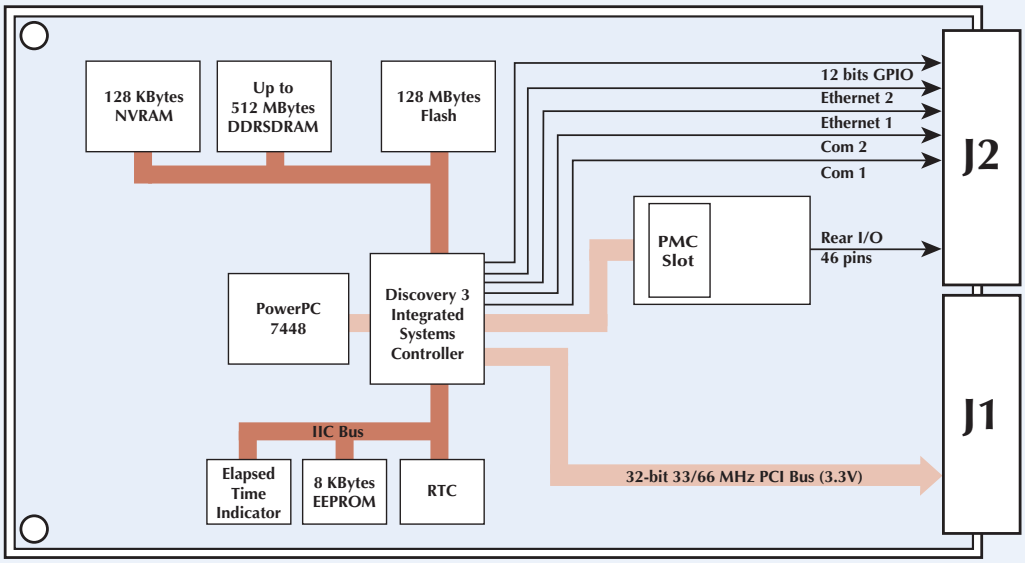
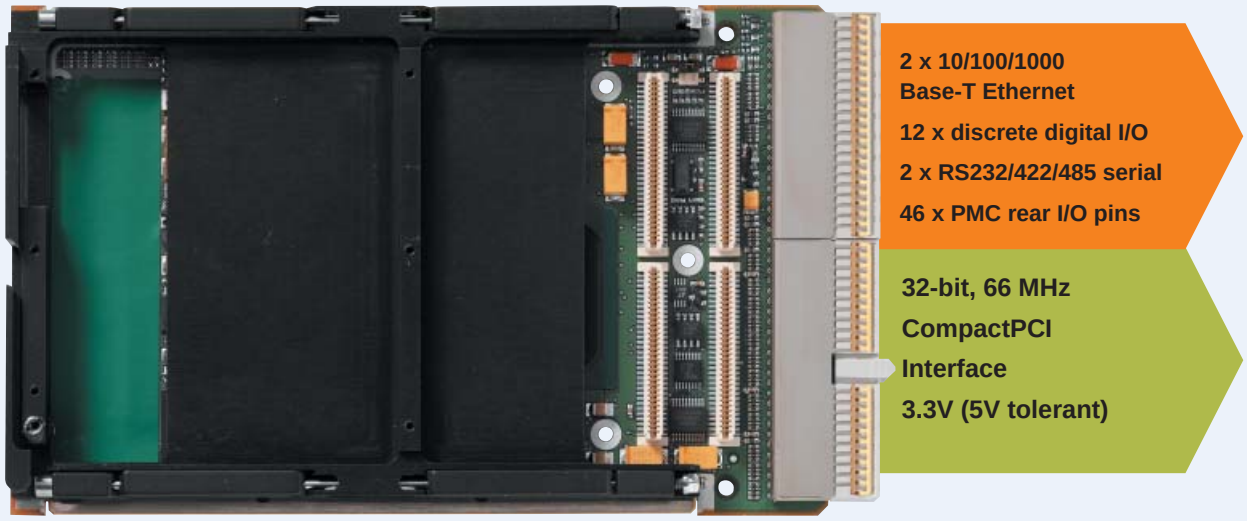


Figure 1: IMP2A Functional Block Diagram

Software Support

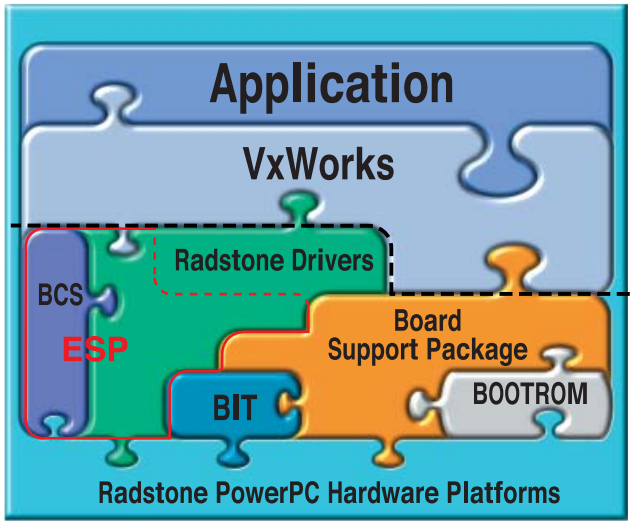
VxWorks provision includes board support packages (BSPs) designed to strict WindRiver definitions, for supporting all defined hardware-related features within VxWorks 5.x and the new VxWorks6 (with memory protection). Enhanced support packages (ESPs), provide extra hardware-related support that is not defined by the operating system vendor (and therefore possesses Radstone interfaces). BSP initialization includes a full PCIbus scan, which will configure the Memory and I/O space of all PCI devices, including any PMC plugged into IMP2A, or any further PMCs on IMPCC1 carriers. For smooth technology insertion, the same BSP/ESP/Deployed Test code modules run both the IMP2A, and its predecessor in our PowerPact3 family, the IMP1A.

ESPs for both VxWorks 5.x and VxWorks6 include a software DMA engine, therefore allowing users to avoid direct and complex hardware programming of this function, plus synchronous serial support and also BCS (see below).



	Ethernet 1	Ethernet 2	Serial 1	Serial 2	Discrete digital I/0
Option 0	10/100	10/100	RS232	RS232/422/485; async only	12 bits
Option 1	10/100	No	RS232/422/485; async/sync	RS232/422/485; async/sync	None
Option 2	10/100	No	RS232	RS232/422/485; async/sync	8 bits
Option 3	10/100	10/100	RS232/422/485; async only	RS232/422/485; async only	8 bits
Option 4	10/100/1000	10/100/1000	RS232	RS232/422/485; async only	4 bits
Option 5	10/100/1000	No	RS232	RS232/422/485; async/sync	4 bits

Figure 2: IMP2A Input/Output Options



Two Deployed Test software modules are available, together providing an overall test philosophy adapted to COTS silicon and COTS operating systems that we believe is unbeaten in the industry.

BIT is supplied as an independent module that runs at initialization, achieving the highest possible coverage by the use of destructive (in system-state terms) testing, before passing control to the operating system. In addition to visual failure indication, the application can read BIT results from Flash.

Background condition screening (BCS) is supplied as part of the ESP, providing continuous, non-destructive testing for early warning of problems while the application is actually running. BCS runs as a task thread and is specifically designed for co-operation with the VxWorks operating system. Both Deployed Test software modules have a broad range of configuration options.

Similar BSP/ESP support to above is available for LynxOS from LynuxWorks. LynxOS is a hard real-time Unix with full memory-management support. It conforms to full POSIX standards and features hard real-time determinism; complete MMU-based protected address spaces for tasks; Linux application binary interface (ABI) personality; Linux binaries that run unchanged on LynxOS v4.0 and above; and true linear scalability. For smooth technology insertion, the same LynxOS BSP/ESP modules run both the IMP2A and its predecessor in the PowerPact3 family, the IMP1A

Support for INTEGRITY on IMP2A is also available direct from our technology partner Green Hills Software Inc. INTEGRITY is a real-time operating system (RTOS) providing secure, maximum reliability operation for use in mission-critical embedded systems.

The royalty-free INTEGRITY RTOS uses hardware memory protection to isolate and protect itself, and user tasks, from incorrect operation caused by accidental errors or malicious tampering. Without the burden of compatibility with 1980s vintage products, INTEGRITY was designed from the ground up for 32-bit and 64-bit embedded processors, and employs the latest in RTOS technology.

Standard Ordering Information

Sales Code	Description
IMP2A-121140x	1.4 GHz PowerPC 7448 3U cPCI SBC, Level 1; 256 MBytes SDRAM, 1 MByte on-chip L2 Cache, 128 MBytes Flash, 2x10/100/1000 Base-T Ethernet ports, 1 x RS232 port, 1 x RS232/422/485 async port, 4 bits GPIO, PCI-x capable PMC slot
IMP2A-221140x	Air-cooled Level 2 as above with conformal coating
IMP2A-321140x	Air-cooled Level 2 as above with conformal coating
IMP2A-421140x	Conduction-cooled Level 4 as above
IMP2A-521140x	Conduction-cooled Level 5 as above

x=software option

NOTE: The standard ordering information (above) defines the standard build variant. Consult your local Radstone sales office for availability of further build options.

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